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| 10/523,257 | 01/27/2005 | Elstan Anthony Fernandez | 2002 P 05725 US | 8306 |

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| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/523,257 | FERNANDEZ, ELSTAN ANTHONY | |
| | Examiner | Art Unit | |
| | Thanh Y. Tran | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/27/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, 7-11, 14-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohki et al (U.S. 6,143,590).

As to claim 1, Ohki et al discloses in figures 12-13 a semiconductor package including a substrate ("motherboard" 257), an integrated circuit ("CPU chip" 232-1) mounted on the substrate (257), and a heat conductive plate (comprising elements 231& 237) having a portion interposed between the integrated circuit ("CPU chip" 232-1) and the substrate (257), the heat conductive plate (231 & 237) being heat-conductively connected to the integrated circuit ("CPU chip" 232-1) and having at least one portion (as indicated at 237) extending laterally out from between the integrated circuit (232-1) and the substrate (257).

As to claim 2, Ohki et al discloses in figures 12-13 a semiconductor package in which the integrated circuit (232-1) is encased in resin (235), the plate (231 & 237) extending out of the resin (235), whereby heat generated in the integrated circuit (232-1) is conducted out of the resin (235).

As to claim 4, Ohki et al discloses in figures 12-13 a semiconductor package, wherein the integrated circuit (232-1) has a substantially square or rectangular profile and where at least one

of the arms (as indicated at 237) extends in a direction which is diagonal relative to the square or rectangular profile of the integrated circuit (232-1).

As to claim 7, Ohki et al discloses in figures 12-13 a semiconductor package, further comprising: a second integrated circuit ("chip" 232-3/232-4) disposed between the plate (231 & 237) and the substrate (257).

As to claim 8, Ohki et al discloses in figures 12-13 a semiconductor package, in which the plate (231 & 237) is in heat-conductive contact to the second integrated circuit ("chip" 232-3/232-4), whereby heat generated by the second integrated circuit ("chip" 232-3/232-4) is conducted away from the second integrated circuit ("chip" 232-3/232-4) by the plate (231/(240-242)).

As to claim 9, Ohki et al discloses in figures 12-13 a semiconductor package in which the second integrated circuit ("chip" 232-3/232-4) is a flipchip.

As to claim 10, Ohki et al discloses in figures 12-13 a semiconductor package and a corresponding method comprising: securing a heat-conductive plate (comprising elements 231 & 237) over a substrate ("motherboard" 257), and mounting at least one integrated circuit ("CPU chip" 232-1) over the heat-conductive plate (231 & 237) with a heat-conductive connection therebetween, the heat conductive plate (231 & 237) having at least one portion (as indicated at 237) extending laterally out from between the integrated circuit (232-1) and the substrate (257).

As to claim 11, Ohki et al discloses in figures 12-13 a semiconductor package and a corresponding method, in which after mounting the integrated circuit (232-1) to the heat-conductive plate (231 & 237), the integrated circuit (232-1) is embedded in resin (235), the heat-conductive plate (231 & 237) extending laterally out of the resin (235).

As to claim 14, Ohki et al discloses in figures 12-13 a packaged semiconductor device comprising: a substrate ("motherboard" 257) including a plurality of contact regions (contacts between lead 237 and substrate 257) on an upper surface; a heat conductive plate (comprising elements 231 & 237) mounted over the substrate (257), the heat conductive plate (231 & 237) comprising a central portion and a plurality of arms (as indicated at 237) extending outwardly from the central portion; an integrated circuit (232-1) having a bottom surface mounted over the central portion of the heat conductive plate (231 & 237); and a plurality of electrical connections (such as 245, 241, 250, and 237) between an upper surface of the integrated circuit (232-1) and the contact regions (where substrate 257 contacts with the leads 237) of the substrate (257), the electrical connections (245, 241, 250, and 237) extending between adjacent ones of the arms (237) of the heat conductive plate (comprising 231 & 237).

As to claim 15, Ohki et al discloses in figures 12-13 a packaged semiconductor device, wherein the heat conductive plate (comprising 231 & 237) further comprises a rim portion ("wiring layer" 241) that surrounds the central portion and is thermally connected to the central portion by the plurality of arms (237). '

As to claim 16, Ohki et al discloses in figures 12-13 a packaged semiconductor device, wherein the heat conductive plate (comprising 231 & 237) includes four diagonal arms (237), each diagonal arm (237) extending outwardly from a corner of the central portion to the rim portion (241).

As to claim 17, Ohki et al discloses in figures 12-13 a packaged semiconductor device, wherein the heat conductive plate (comprising 231 & 237) further includes four lateral arms (figure 13 discloses at least four lateral arms 237), each lateral arm (237) extending outwardly

from a side surface of the central portion of the plate (comprising 231 & 237) to the rim portion (241).

As to claim 18, Ohki et al discloses in figures 12-13 a packaged semiconductor device, wherein the electrical connections (such as 245, 241, 250, and 237) comprise wire bonds (250).

As to claim 20, Ohki et al discloses in figures 12-13 a packaged semiconductor device, wherein the central portion of the heat conductive plate (comprising 231 & 237) is affixed to the integrated circuit (232-1) by heat-conductive glue (bumps 245) and wherein the central portion of the heat conductive plate (comprising 231 & 237) is affixed to the substrate (257) by heat-conductive glue ("soldering") (see col. 15, lines 12-13; and col. 17, lines 60-65).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohki et al (U.S. 6,143,590) in view of Moden (U.S. 6,303,981).

As to claim 3, Ohki et al discloses in figures 12-13 a semiconductor package in which the plate (241 and 237) includes a central region disposed between the substrate (240) and the integrated circuit (232-1) and arms (as indicated at 237) extending laterally from the central region with openings between them (see the openings between the central region and the arms of plate 241, 237).

Ohki et al does not disclose the integrated circuit being connected to the substrate by wire bonding in the openings.

Moden discloses in figure 2A a semiconductor package comprising an integrated circuit ("die" 16A) being connected to the substrate ("lead frame segment" 18B) by wire bonding ("bond wires" 36A) in the openings (openings of 18A and 18B). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Ohki et al by having the integrated circuit is connected to the substrate by wire bonding in the openings Moden for providing an electrical connection between the chip and the substrate in the semiconductor package.

As to claim 13, Ohki et al discloses in figures 12-13 a semiconductor package and a corresponding method in which there are a plurality of said integrated circuits (232-1, 232-2, 232-3 and 232-4), the plate (231 & 237) extending between each of the integrated circuits (232-1, 232-2, 232-3 and 232-4) and the substrate (257).

Ohki et al does not disclose the method further including a singulation step in which the substrate and plate are cut to produce a plurality of semiconductor packages each including at least one of the integrated circuits.

Moden discloses in figures 4A-4E a semiconductor package and a corresponding method comprising: a singulation step in which the substrate ("second leadframe" 28B) and plate ("leadframe" 28A) are cut to produce a plurality of semiconductor packages (figures 4D-4E) each including at least one of the integrated circuits ("semiconductor dice" 16A). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Ohki et al by having a singulation step in which

the substrate and plate are cut to produce a plurality of semiconductor packages each including at least one of the integrated circuits as taught by Moden for providing a plurality of semiconductor packages.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohki et al (U.S. 6,143,590) in view of Ohsawa et al (U.S. 2002/0031862).

As to claim 6, Ohki et al does not disclose the plate includes at least one portion of increased thickness laterally outward from the integrated circuit.

Ohsawa et al discloses in figures 2A-2D a semiconductor package comprising a plate (comprising elements 2 and 3) includes at least one portion (3) of increased thickness laterally outward from the integrated circuit ("LSI chip" 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Ohki et al by having a plate that includes at least one portion of increased thickness laterally outward from the integrated circuit as taught by Ohsawa et al for supporting the semiconductor package when the semiconductor package is mounted a motherboard.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohki et al (U.S. 6,143,590) in view of Joshi (U.S. 4,069,498).

As to claim 5, Ohki et al does not disclose the plate is grounded and electrically connected to at least one ground input of the integrated circuit.

Joshi discloses in column 1, lines 36-39 a heat plate is grounded ("ground potential") and electrically connected to at least one ground input of the integrated circuit ("chip"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Ohki et al by having a heat plate is grounded and electrically connected to at least one ground input of the integrated circuit as taught by Joshi for providing a good heat mechanism or good electrical conductors, and enhancing the heat transfer from the chip (col. 1, lines 45-68 in Joshi)

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohki et al (U.S. 6,143,590) in view of Papageorge et al (U.S. 5,438,224).

As to claim 19, Ohki et al does not disclose a plurality of balls disposed on a lower surface of the substrate, each of the balls electrically coupled to a respective one of the contact regions.

Papageorge et al discloses in figure 1 a packaged semiconductor device comprising: a plurality of balls ("bumps" 159 disposed on a lower surface of the substrate (150), each of the balls (159) electrically coupled to a respective one of the contact regions (152). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohki et al by having a plurality of balls disposed on a lower surface of the substrate, each of the balls electrically coupled to a respective one of the contact regions as taught by Papageorge et al for coupling the IC assembly or semiconductor package to circuitry of the external circuit board (see col. 5, lines 40-53 in Papageorge et al).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohki et al (U.S. 6,143,590) in view of Sano et al (U.S. 5,952,714).

As to claim 12, Ohki et al does not disclose a semiconductor package in which prior to securing the heat-conductive plate to the substrate a second integrated circuit is mounted on the substrate, the heat-conductive plate being secured to the substrate with the second integrated circuit between a portion of the plate and the substrate.

Sano et al discloses in figure 5 a semiconductor package and a corresponding method in which prior to securing the heat-conductive plate ("lead frame" 24) to the substrate (42) a second integrated circuit ("chip" 41) is mounted on the substrate (42), the heat-conductive plate (24) being secured to the substrate (42) with the second integrated circuit (41) between a portion of the plate (24) and the substrate (24). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Ohki et al by having the step of: prior to securing the heat-conductive plate to the substrate a second integrated circuit is mounted on the substrate, the heat-conductive plate being secured to the substrate with the second integrated circuit between a portion of the plate and the substrate as taught by Sano et al for providing an easy assembling process for the semiconductor package.

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akram (U.S. 6,297,547) and Venkateshwaran et al (U.S. 6,388,336) disclose relevant prior art to the present invention.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
21 June 2006